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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/637,500	08/11/2000	Robert Gelinas	07030.0011-00	7608

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EXAMINER

TSAL, HENRY

ART UNIT	PAPER NUMBER
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2183

DATE MAILED: 04/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/637,500

Applicant(s)

GELINAS ET AL.

Examiner

Henry W.H. Tsai

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 March 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5 and 11-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5 and 11-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s) _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

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DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-3, 11-20, 23 and 24 are rejected under 35 U.S.C. 102(e) as being anticipated by Agarwal et al. (U.S. Patent No. 6,308,252), hereafter referred to as Agarwal et al.'252.

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Referring to claim 1, Agarwal et al.'252 discloses, as claimed, a digital signal processor (100, see Figs. 1 and 3) comprising: two execution pipelines (first pipeline 314 and second pipeline 316, see Fig. 3) capable of executing RISC (the instructions delivered to the first pipeline 314, see Col. 6, lines 17-19) and DSP instructions (the instructions delivered to the second pipeline 316, see Col. 6, lines 19-21); instruction fetch logic (instruction fetch unit 310, see Fig. 5) that simultaneously fetches (see Col. 4, line 19-20, and Col. 6, lines 8-9, regarding two instructions are issued simultaneously from the instruction fetch unit 310) two instructions and routes them to respective pipelines (first pipeline 314 and second pipeline 316, see Fig. 3); and control logic (312, see Fig. 3 and Col. 7, lines 34-36) to allow the pipelines to operate independently (as shown in Fig. 3, the first pipeline 314 and second pipelines 316 operate the instructions independently). Note the instructions shown in Col. 4 and Col. 5 can be interpreted as a RISC instruction or a DSP instruction since they can be used in a RISC system or a regular digital signal processing system.

Referring to claim 13, Agarwal et al.'252 discloses, as claimed, a method for processing instructions in a digital signal processor (100, see Figs. 1 and 3), the method comprising: simultaneously fetching (see Col. 4, line 19-20, and Col. 6,

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lines 8-9, regarding two instructions are issued simultaneously from the instruction fetch unit 310) a first instruction (the instructions delivered to the first pipeline 314, see Col. 6, lines 17-19) and a second instruction (the instructions delivered to the second pipeline 316, see Col. 6, lines 19-21); routing the first instruction to a first execution pipeline (first pipeline 314) and the second instruction to a second execution pipeline (second pipeline 316), wherein the first execution pipeline and the second execution pipeline are capable of executing RISC and DSP instructions (see Col. 6, lines 21-24, regarding the instructions delivered to the first pipeline 314 can also be delivered to the second pipeline 316 since each pipeline has an integer unit (320 or 324), see Fig. 3); and using control logic (312, see Fig. 3 and Col.7, lines 34-36) to operate the first execution pipeline and the second execution pipeline independently (as shown in Fig. 3, the first pipeline 314 and second pipelines 316 operate the instructions independently).

Referring to claim 18, Agarwal et al.'252 discloses, as claimed, a system (see Figs. 1 and 3) for processing instructions, comprising: an instruction memory (such as main memory or instruction cache memory in the Agarwal et al.'252's system) having instructions; and a digital signal processor (100 or 300, see Figs. 1 and 3) that includes: two execution pipelines

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(first pipeline 314 and second pipeline 316, see Fig. 3) capable of executing RISC (such as the instructions need to use floating point unit see Col. 6, lines 17-19) and DSP (the instructions need to use load/store unit 326 or coprocessor 328, see Col. 6, lines 19-21) instructions; instruction fetch logic (instruction fetch unit 310, see Fig. 5) that simultaneously fetches (see Col. 4, line 19-20, and Col. 6, lines 8-9, regarding two instructions are issued simultaneously from the instruction fetch unit 310) two instructions from the instruction memory (such as main memory or instruction cache memory in the Agarwal et al.'252's system) and routes them to respective pipelines; and control logic (312, see Fig. 3 and Col.7, lines 34-36) to allow the pipelines to operate independently (as shown in Fig. 3, the first pipeline 314 and second pipelines 316 operate the instructions independently). Note the instructions shown in Col. 4 and Col. 5 can be interpreted as a RISC instruction or a DSP instruction since they can be used in a RISC system or a regular digital signal processing system.

As to claims 2, 14, and 19, Agarwal et al.'252 also discloses: the instruction fetch logic (instruction fetch unit 310, see Fig. 3) includes logic that fetches dual SIMD instructions (see Col. 4, line 19-25, Col. 5, lines 50-51, and Col. 6, lines 8-10).

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As to claims 3, 15, and 20, Agarwal et al.'252 also discloses two registers (311a and 311b, see Fig. 5) each half the length of a word (broadly interpreted since a word length was not well defined) fetched for memory, and the instruction fetch logic (instruction fetch unit 310, see Fig. 5) that fetches a single word into the two registers (311a and 311b, see Fig. 5) simultaneously.

As to claims 11, 16, and 23, Agarwal et al.'252 also discloses each of the two execution pipelines is capable of executing both RISC and DSP instructions (see Col. 6, lines 21-24, regarding the instructions delivered to the first pipeline 314 can also be delivered to the second pipeline 316 since each pipeline has an integer unit (320 or 324), see Fig. 3).

As to claims 12, 17, and 24, Agarwal et al.'252 also discloses one (the first pipeline 314) of the execution pipelines is dedicated to processing RISC instructions (the instructions need to use floating point unit see Col. 6, lines 17-19) and one (the second pipeline 316) of the execution pipelines is dedicated to processing DSP instructions (the instructions need to use load/store unit 326 or coprocessor 328, see Col. 6, lines 19-21).

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Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4, 5, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal et al.'252 in view of Chuang (U.S. Patent No. 4,766,566), hereafter referred to as Chuang'566.

Agarwal et al.'252 discloses the claimed invention except for: explicitly showing to use an eight port general register file (claims 4 and 21) and the general register file including four read registers and four write registers (claims 5 and 22).

Chuang'566 discloses an eight port general register file (48, see Fig. 2); and the general register file including three read registers and five write registers (48, see Fig. 2).

However, the number of the read and write registers are changeable as required in practice.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Agarwal et

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al.'252's system to comprise: an eight port general register file; and the general register file including four read registers and four write registers, as taught by Chuang'566, in order to facilitate reading and writing the data efficiently for the Agarwal et al.'252's system. Besides, the number of the read and write registers are changeable as required in practice.

Further, as shown in re Rose, 105 USPQ 237 (CCPA 1955), to make changes in size/range generally does not provide patentable weight to the claimed invention.

Response to Amendment

5. Applicant's arguments filed 3/8/05 have been fully considered but they are not deemed to be persuasive.

Applicants argue that "Agarwal does not describe or suggest two execution pipelines capable of executing RISC and DSP instructions. Instead, Agarwal describes pipelines that are only capable of executing RISC instructions. Agarwal does not describe a digital signal processor that includes two execution pipelines that are capable of executing RISC and DSP instructions." (page 6, lines 19-22) Examiner disagrees with Applicants. As set forth in the are rejections above, Agarwal et al.'252 discloses, as claimed, a digital signal processor

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(100, see Figs. 1 and 3) comprising: two execution pipelines (first pipeline 314 and second pipeline 316, see Fig. 3) capable of executing RISC (the instructions delivered to the first pipeline 314, see Col. 6, lines 17-19) and DSP instructions (the instructions delivered to the second pipeline 316, see Col. 6, lines 19-21). Note the instructions shown in Col. 4 and Col. 5 can be interpreted as a RISC instruction or a DSP instruction since they can be used in a RISC system or a regular digital signal processing system.

Applicants further argue that "Chuang does not remedy the failure of Agarwal to describe or suggest a digital signal processor that includes two execution pipelines that are capable of executing RISC and DSP instructions, as recited in amended claim 1, from which claims 4 and 5 depend." (page 7, lines 1-3) Examiner disagrees with Applicants. Again, as set forth in the are rejections above, Agarwal et al.'252 discloses, as claimed, a digital signal processor (100, see Figs. 1 and 3) comprising: two execution pipelines (first pipeline 314 and second pipeline 316, see Fig. 3) capable of executing RISC (the instructions delivered to the first pipeline 314, see Col. 6, lines 17-19) and DSP instructions (the instructions delivered to the second pipeline 316, see Col. 6, lines 19-21). Note the instructions

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shown in Col. 4 and Col. 5 can be interpreted as a RISC instruction or a DSP instruction since they can be used in a RISC system or a regular digital signal processing system.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kiuchi et al.'524 discloses digital signal processor and method for executing DSP and RISC class instructions defining identical data processing or data transfer operations. The system is also capable of executing RISC and DSP instructions as claimed.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

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extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (571) 272-4176. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (571) 272-4162. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the TC central telephone number, 571-272-2100.

9. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into the Group at fax number: 703-872-9306. This practice may be used for filing papers not requiring a fee. It

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may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

A handwritten signature in black ink, appearing to read "Henry Tsai", with a stylized flourish at the end.

HENRY W. H. TSAI
PRIMARY EXAMINER

April 27, 2005